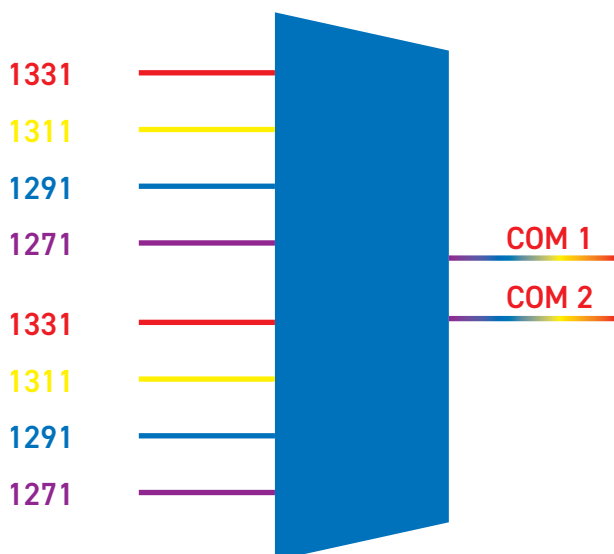




2x400G CWDM4 MUX CHIP on Wafer/Stripe

1. DESCRIPTION

Product Function



Product Application:

The specifications serve for CWDM MUX in WDM system.

2. OPTIC SPECIFICATION

NO.	PARAMETER	SPECIFICATION			UNITS	NOTE
		MIN.	TYP.	MAX.		
2.1	Channels	4			Ch	
2.2	Channel Spacing	20			nm	
2.3	Center wavelength		1271		nm	reference grid
			1291			
			1311			
			1331			
2.4	Wavelength Accuracy	-1		1	nm	Offset from reference grid
2.5	1dB Bandwidth	10			nm	1dB from peak transmission, gross bandwidth, average polarization. For each channel.
2.6	3dB Bandwidth	14			nm	3dB from peak transmission, gross bandwidth, average polarization. For each channel.
2.7	Insertion Loss			2.5	dB	Defined as the average polarization, at reference grid $\pm$ 4nm.
2.8	Insertion Loss Uniformity			1.0	dB	Loss uniformity among channels at reference grid $\pm$ 4nm.
2.9	Polarization Dependent Loss			0.5	dB	Maximum insertion loss difference between all polarization within reference grid $\pm$ 1nm.

Note: Specification must be met under room temperature test.

3. ABSOLUTE MAXIMUM RATINGS

NO.	PARAMETERS	SPECIFICATIONS	UNIT	NOTES
3.1	Operating temperature	-5 ~ +75	°C	
3.3	Storage Temperature	-40 ~ +85	°C	

4. ENVIRONMENTAL SAFETY

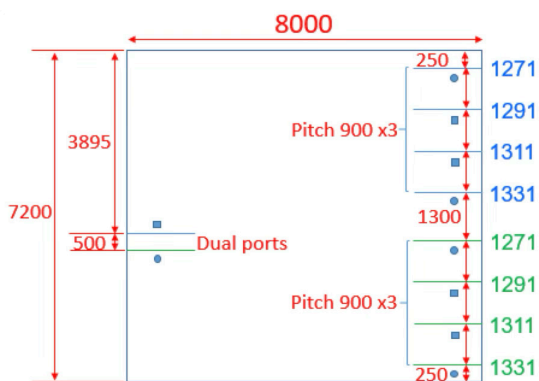
Compliant to ROHS10

5. MUX CHIP DIMENSION

TYPE	DIMENSION	PITCH
MUX	8.0x7.2x0.67mm	900um

NOTE

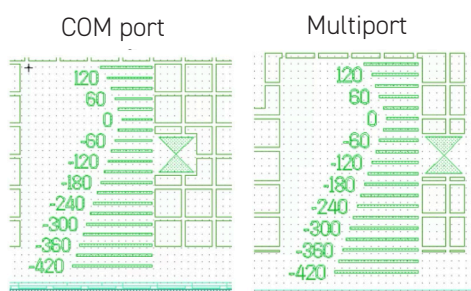
- This dimension is final size after chip dicing and polishing.
- Common port is mode-matching with SMF.
- Multi-ports are mode-matching with SMF.



Polishing illustration:

Polishing Line:

Polishing must stop before zero tick mark

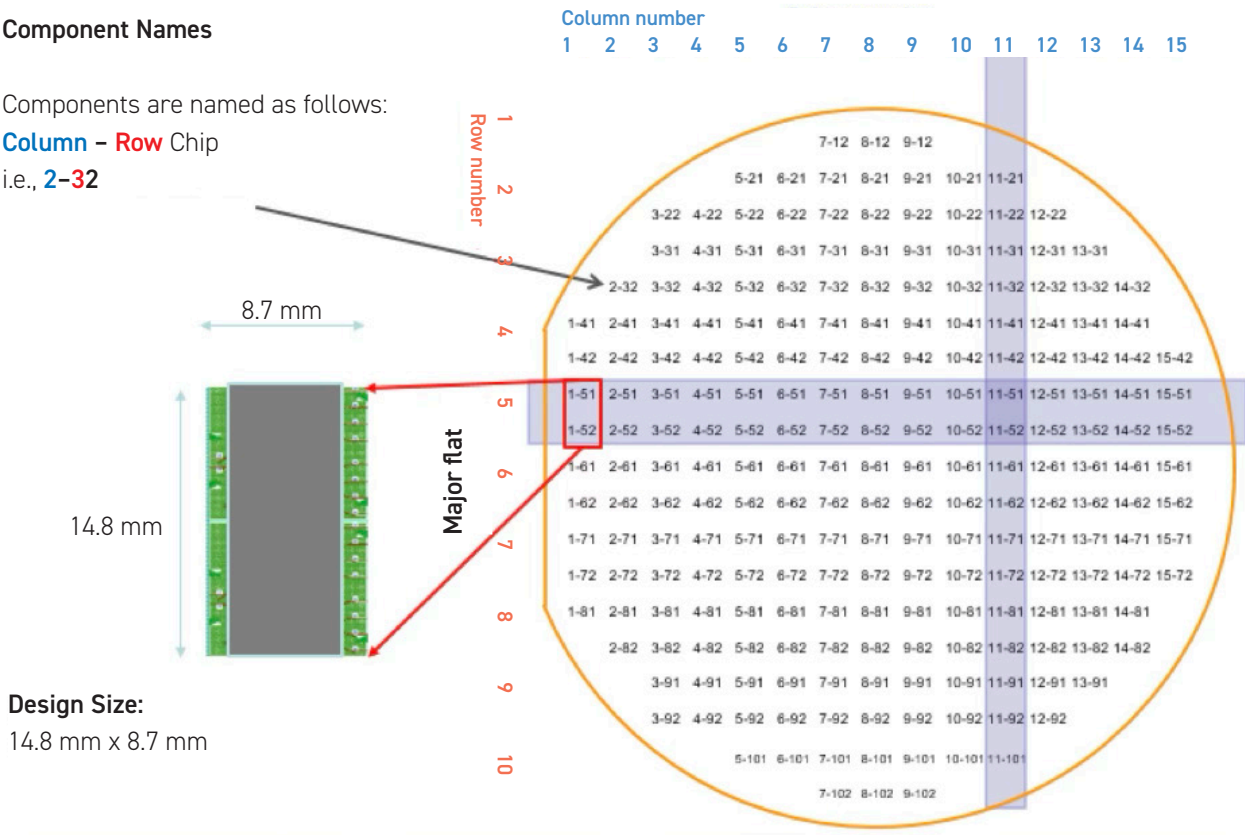


6. MUX Wafer Information

Component Names

Components are named as follows:

Column - **Row** Chip
i.e., **2-32**



Design Size:

14.8 mm x 8.7 mm

Stripe No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Total
Number	9	11	15	15	17	17	19	10	19	17	17	15	13	11	7	221

7. QUALITY CONTROL

Stripes: On each Mux, there are control channels for screening. Failed Mux chips will be noted.

Wafers: In each batch a wafer will be selected for control screening. Control screening means optical measurement of through control channels in chips on at least 2 stripes. The control screening will ensure that the wafers in the batch will have yields of >90%.