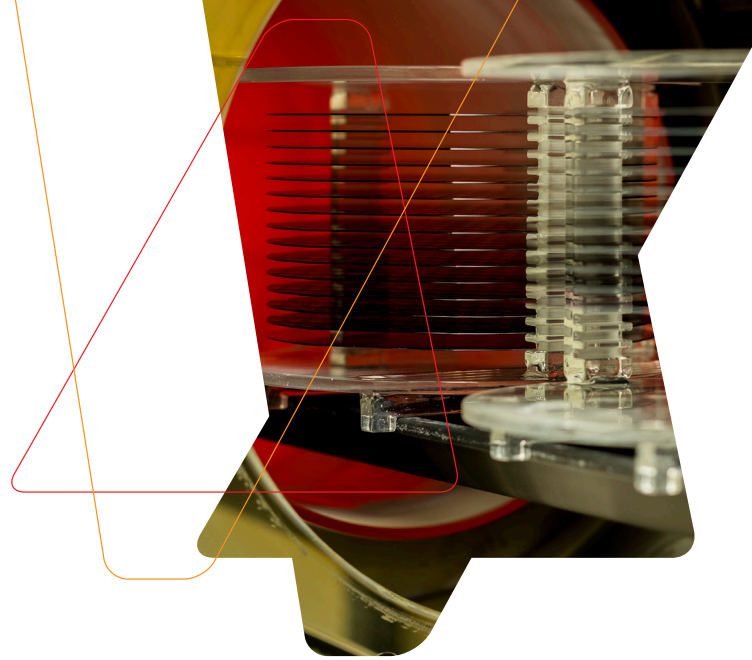
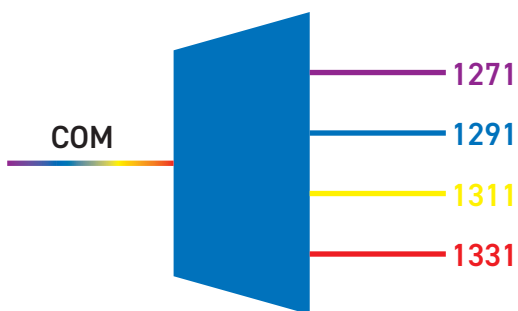




CWDM4 DEMUX CHIP on Wafer/Stripe (250pitch)

1. DESCRIPTION

Product Function:



Product Application:

The specifications serve for CWDM DEMUX in WDM system.

2. OPTIC SPECIFICATION

NO.	PARAMETER	SPECIFICATION			UNITS	NOTE
		MIN.	TYP.	MAX.		
2.1	Channels	4			Ch	
2.2	Channel Spacing	20			nm	
2.3	Center wavelength		1271		nm	at ITU grid
			1291			
			1311			
			1331			
2.4	Wavelength Accuracy	-1		1	nm	Offset from ITU grid
2.5	1dB Bandwidth	12.5			nm	1dB from peak transmission, gross bandwidth, average case polarization. For each channel.
2.6	3dB Bandwidth	15			nm	3dB from peak transmission, gross bandwidth, average case polarization. For each channel.
2.7	Insertion Loss1 (class A)			1.6	dB	Defined as the average case polarization, at ITU±2nm.
2.8	Insertion Loss2 (class B)			2.0	dB	Defined as the average case polarization, at ITU±2nm.
2.9	Insertion Loss Uniformity			1.0	dB	Loss uniformity among channels at ITU±2nm.
2.10	Polarization Dependent Loss			0.5	dB	Maximum insertion loss difference between all polarization within ITU±1nm.
2.11	Adjacent Channel Isolation	20			dB	Insertion loss to the maximum transmission across ±6.5nm around the adjacent ITU wavelength λ _{ITU} , for each port, for average polarization.

3. ABSOLUTE MAXIMUM RATINGS

NO.	PARAMETERS	SPECIFICATIONS	UNIT	NOTES
3.1	Operating Temperature	-5 ~ +75	°C	
3.3	Storage Temperature	-40 ~ +85	°C	

4. ENVIRONMENTAL SAFETY

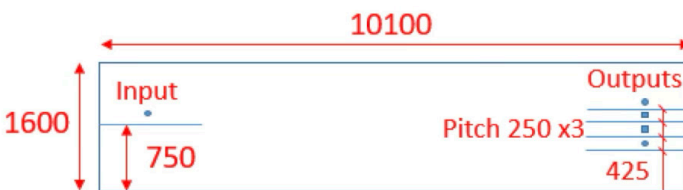
Compliant to ROHS10

5. AWG CHIP DIMENSION

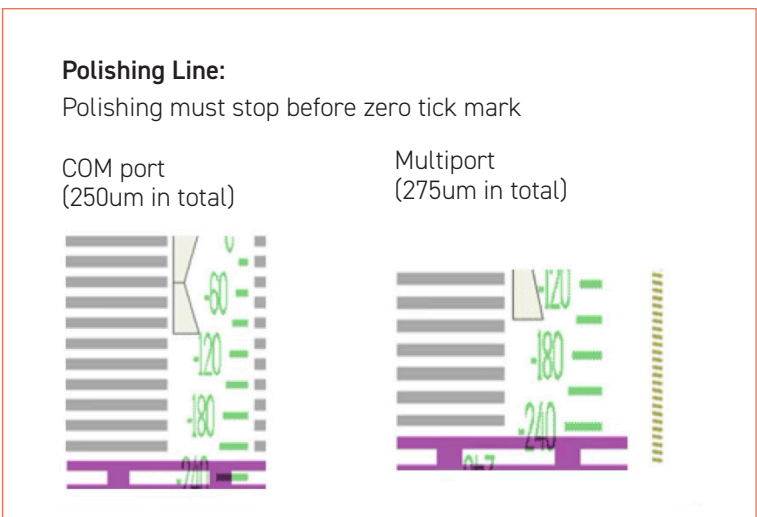
TYPE	DIMENSION	PITCH
DEMUX	10.1x1.6x0.67mm	250um

NOTE

- This dimension is final size after chip dicing and polishing.
- Common port is mode-matching with SMF.
- Multi-ports are multimode waveguides. The mode field dimension is around 5um x 15um.



Polishing illustration:

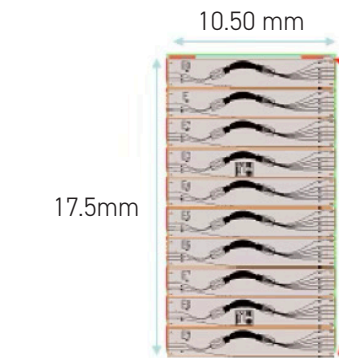


6. DEMUX Wafer/Stripe Information

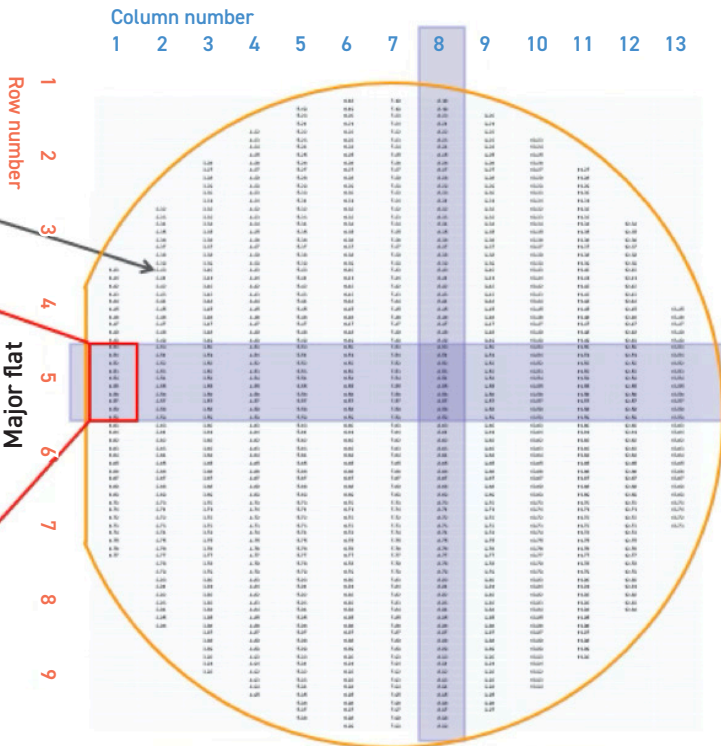
Component Names

Components are named as follows:

Column – **Row** Chip
i.e., **2-40**



Design Size:
17.5mm x 10.50mm



Stripe No.	1	2	3	4	5	6	7	8	9	10	11	12	13	Total
Number	38	55	67	74	80	82	82	82	78	72	64	51	29	854

7. QUALITY CONTROL

Stripes: On each Demux, there are control channels for screening. Failed Demux chips will be noted.

Wafers: In each batch a wafer will be selected for control screening. Control screening means optical measurement of through control channels in chips on least 2 stripes. The control screening will ensure that the wafers in the batch will have yields of >90%.